ABSTRACT OF THE DISCLOSURE

In an image processing apparatus which performs first and second operations, a first processor processes image data in correspondence to the first operation, while a second processor which processes image data in correspondence to the second operation. Further, a memory is shared by the first and second processors. A controller connects the first processor to the memory in the first operation and to connect the second processor to the memory in the second operation. For example, the above-mentioned first and second processors are constructed by a common device such as a field gate programmable array wherein a function thereof can be rewritten.